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(54) Semiconductor device comprising a capacitor and method of manufacturing the same

(57) A semiconductor device has a device isolation oxide film, an interlayer insulating film, hydrogen barrier films, a lower electrode, a capacitor insulating film, an upper electrode, an interlayer insulating film and a wiring layer, formed on a silicon substrate. A gate electrode is formed on a gate oxide film between impurity diffusion regions in the silicon substrate. Further, a capacitor portion, comprising the lower electrode, the capacitor insulating film (ferroelectric or high dielectric substance) and the upper electrode, is completely covered with the hydrogen barrier films. The hydrogen barrier films prevent deterioration of the ferroelectric substance and the high dielectric constant material due to reducing conditions in a hydrogen atmosphere. Other device characteristics, however, are not adversely affected because only the capacitor portion is completely covered with the hydrogen barrier films.

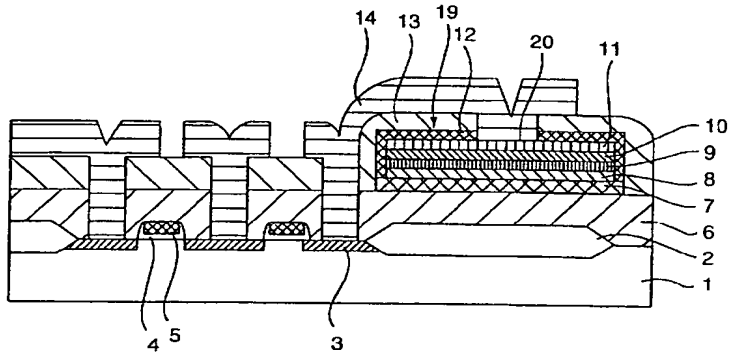

FIG. 1

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a semiconductor device in which a ferroelectric substance material or a high dielectric constant material is mainly used as a capacitor insulating film and a method of manufacturing the same.

2. Statement of the Problem

[0002] Recently, development has been made in the area of semiconductor devices concerning a non-volatile memory having a capacitor device region in which a ferroelectric substance material, such as $Pb(Zr,Ti)O_3$ and $SrBi_2Ta_2O_9$, having a hysteresis characteristic is used as a capacitor insulating film, and concerning a dynamic random access memory in which a capacitor device region has a large quantity of stored electric charges by using a high dielectric substance material, such as $(Sr,Ba)TiO_3$, as the capacitor insulating film.

[0003] It has been known that deterioration of an insulating characteristic and a ferroelectric characteristic occurs in the dielectric substance, such as $Pb(Zr,Ti)O_3$ and $(Sr,Ba)TiO_3$, used in the above semiconductor device, when the dielectric substance is subjected to a reduction atmosphere because the dielectric substance is formed by an oxide. In particular, when the dielectric substance is exposed to hydrogen, the device characteristics deteriorate critically. In the extreme case, peeling of an electrode may be caused to occur.

[0004] However, a hydrogen atmosphere inevitably is produced in a manufacturing process of the semiconductor device, such as a large scale integrated circuit ("LSI"). For example, a SiO_2 film which is used as an interlayer insulating film is generally formed by the use of a chemical vapor deposition ("CVD") method. The reaction is represented by

$$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2.$$

This reaction formula indicates that the hydrogen is generated as a reaction product. Further, the CVD of tungsten ("W") tends to be widely used to embed a contact hole having a large aspect ratio as the device size becomes small. In this case, the W is deposited by the reaction which is represented by

$$2WF_6 + 3SiH_4 \rightarrow 2W + 3SiH_4 + 6H_2.$$

This reaction formula indicates that the reaction is carried out in a very strong reduction atmosphere. In addition, an annealing process is performed in an atmosphere containing the hydrogen to ensure the characteristic of a MOS transistor after the formation of an Al wiring pattern.

[0005] Means for preventing the dielectric capacitor from deteriorating due to the hydrogen has been adopted in several semiconductor devices, as known in the art. For example, disclosure is made in Japanese Unexamined Patent Publication No. H4-102367 of a semiconductor device, illustrated in FIG. 27, which has a TiN film or a TiON film formed on an interlayer insulating film 16 of a capacitor portion 19 as a hydrogen barrier film 17. In the structure illustrated in FIG. 27, a device isolation oxide film 2, an interlayer insulating film 6, a lower electrode 8, a capacitor insulating film 9, an upper electrode 10, an interlayer insulating film 13, a wiring layer 14, an interlayer insulating film 16, and a hydrogen barrier film 17 are successively deposited on a silicon substrate 1 in this order. Further, a gate electrode 5 is formed on a gate oxide film 4 between impurity diffusion regions 3 in the silicon substrate 1.

[0006] Alternatively, AlN or Ti_3N_4 is formed on an upper electrode 10 of a capacitor portion 19 as a hydrogen barrier film 11 in the structure illustrated in FIG. 28 in the case of a dielectric memory which is disclosed in Japanese Unexamined Patent Publication No. H7-111318. On the other hand, Si_3N_4 is formed on the entire surface of the device as a hydrogen barrier film 12 in the structure illustrated in FIG. 29.

[0007] More specifically, a device isolation oxide film 2, an interlayer insulating film 6, a lower electrode 8, a capacitor insulating film 9, an upper electrode 10, a hydrogen barrier film 11, an interlayer insulating film 13 and a wiring layer 14 are successively deposited on a silicon substrate 1 in this order in the structure illustrated in FIG. 28. Further, a gate electrode 5 is formed on a gate oxide film 4 between impurity diffusion regions 3 in the silicon substrate 1. In the structure illustrated in FIG. 29, a device isolation oxide film 2, an interlayer insulating film 6, a lower electrode 8, a capacitor insulating film 9, an upper electrode 10, a hydrogen barrier film 11, a hydrogen barrier film 12, an interlayer insulating film 13 and a wiring layer 14 are successively deposited on a silicon substrate 1 in this order. In this case, the hydrogen barrier film 12 is formed to cover the lower electrode 8, the capacitor insulating film 9, the upper electrode 10 and the hydrogen barrier film 11. In addition, a gate electrode 5 is formed on a gate oxide film 4 between impurity diffusion regions 3 in the silicon substrate 1.

[0008] Where the hydrogen barrier film 17 is formed on the interlayer insulating film 16 of the capacitor portion 19 like the conventional semiconductor device illustrated in FIG. 27, the hydrogen barrier film 17 must cover the capacitor portion 19 with a space area of several microns or more from the capacitor portion 19 to prevent the invasion of the hydrogen from a lateral direction. However, cell area has been reduced with the high integration of memories, and the cell area of a highly integrated memory of 256 Megabit or more is 1 μm^2 or less, as disclosed in Nikkey Micro Device, March

1995, at page 31. In such a case, the area of the hydrogen barrier film 17 over the capacitor portion 19 must be equal to or less than the cell area. Consequently, the invasion of the hydrogen from the lateral direction cannot sufficiently be prevented. In addition, the conventional semiconductor device is not effective at all for avoiding deterioration of the capacitor portion 19 due to the hydrogen where CVD of W is used for the wiring layer, since the hydrogen barrier film is formed over the wiring layer 14.

[0009] Further, the other conventional semiconductor device illustrated in FIG. 28 is not effective at all for avoiding the invasion of the hydrogen from the side portion. In addition, the characteristic of the MOS transistor which is ensured by the hydrogen anneal is hindered after the formation of the Al wiring pattern in the other conventional semiconductor device illustrated in FIG. 29, since the Si_3N_4 film is formed for the entire surface of the device. In this case, the hindrance of the hydrogen annealing effect from the formation of Si_3N_4 film has been widely known as described in PROCEEDINGS OF THE SYMPOSIUM ON SILICON NITRIDE THIN INSULATING FILMS, 1983, pages 94 to 110.

3. Solution to the Problem

[0010] In the semiconductor device according to this invention, the capacitor portion is directly covered with the hydrogen barrier film and further, the hydrogen barrier film, except for a part covering the capacitor portion, is removed. Consequently, the characteristic of the MOS transistor is not adversely affected, and the deterioration of the capacitor portion can be effectively avoided.

[0011] According to this invention, there is provided a semiconductor device which has a capacitor portion including a ferroelectric substance material or a high dielectric constant material as a capacitor insulating film. The capacitor portion is covered with a hydrogen barrier film, and the remaining portion excepting the capacitor portion is uncovered with the hydrogen barrier film.

[0012] A method of manufacturing the semiconductor device according to this invention includes a step of forming the capacitor portion comprising a lower electrode, a capacitor insulating film of ferroelectric substance material or high dielectric constant material and an upper electrode, a step of forming the hydrogen barrier film for covering the capacitor portion, and a step of removing a part of the hydrogen barrier film by etching.

[0013] A feature of the invention is a semiconductor device having a capacitor portion covered by a hydrogen barrier film, and a portion having no hydrogen barrier film.

[0014] Another feature of the invention is a contact portion on the capacitor portion, formed by removing a portion of hydrogen barrier film from the capacitor portion.

[0015] Another feature of the invention is a nonconductive hydrogen barrier film containing at least one material selected from the group consisting of Si_3N_4, SiON and a combination of Si_3N_4, SiON and SiO_2.

[0016] Another feature of the invention is an electrically conductive hydrogen barrier film comprising at least one material selected from nitrides of the group consisting of Ti, Zr, Nb, Ta, Hf and W.

[0017] Another feature of the invention is the utilization of an electrically conductive hydrogen barrier film as the upper electrode of a memory capacitor.

[0018] In a first basic embodiment, the invention comprises a substrate and a transistor portion having a gate oxide film on the substrate, a gate electrode on the gate oxide film, and an impurity diffusion region in the substrate. It further includes a capacitor portion containing a capacitor insulating film and having a surface. A hydrogen barrier film is located on the surface of the capacitor portion. A contact portion is formed on the surface of the capacitor portion by removing a portion of the hydrogen barrier film from the capacitor portion. The contact portion is for electrically contacting the capacitor portion to the transistor portion. The capacitor portion does not overlap the transistor portion.

[0019] In one variation of the first basic embodiment of the invention, a nonconductive hydrogen barrier film is formed on an interlayer insulating film, then a lower electrode and a capacitor insulating film are formed. Then an upper electrode and a conductive hydrogen barrier, or alternatively just a conductive hydrogen barrier serving also as an electrode, are formed. These films are patterned, and then the patterned surface is covered with a second nonconductive hydrogen barrier film. A contact hole is made in the second nonconductive hydrogen barrier film to form a contact portion on the conductive film below.

[0020] In another variation, the upper electrode is formed on the capacitor insulating film, the films are patterned to form a capacitor, then the second nonconductive hydrogen barrier film is formed to cover the surfaces of the capacitor. Then a portion of the nonconductive hydrogen is removed to form a contact hole and a contact portion on the upper electrode. Then a conductive hydrogen barrier film is formed to fill the contact hole and cover the contact portion and the top of the capacitor portion. Alternatively, an interlayer insulating film can be formed on the second nonconductive hydrogen barrier film, a contact hole made through both the interlayer insulating film and the second nonconductive hydrogen barrier film, and then the contact portion covered with the conductive hydrogen barrier film

[0021] In another second basic embodiment, the invention comprises a substrate and a transistor portion having a gate oxide film on the substrate, a gate electrode on the gate oxide film, and an impurity diffusion region in the substrate. It further includes a plurality of capacitor portions, each having a lower electrode and a capacitor insulating film, each of the capacitor portions

overlapping a transistor portion. Each capacitor portion is located over a plug, which is electrically connected to the transistor portion. A first, nonconductive hydrogen barrier film is formed on an interlayer insulating film. A second, electrically conductive hydrogen barrier film is formed on the first, nonconductive hydrogen barrier film and the plug. A lower electrode is formed on the second, conductive hydrogen barrier film. The lower electrode and the second, conductive hydrogen barrier film are patterned to form a patterned surface. The capacitor insulating film is formed on the patterned surface and then it is removed from the surface except not from the top and side surfaces of the capacitor portion. A third, conductive hydrogen barrier film is formed on the capacitor insulating layer and the first, nonconductive hydrogen barrier film. Then the third, conductive hydrogen barrier film and the first, nonconductive hydrogen barrier film are removed from the underlying interlayer insulating film, but not from the capacitor portion. Thus, the capacitor portions are covered by hydrogen barrier film, but there is a portion between the capacitor portions that is not covered.

[0022] A first variation of the second basic embodiment includes a first, electrically nonconductive hydrogen barrier film formed on the plug and on the interlayer insulating film, as described above, but the capacitor insulating film is patterned in the same process as the third, conductive hydrogen barrier film and the nonconductive hydrogen barrier film. In a second variation, no nonconductive hydrogen barrier film is formed on the interlayer insulating layer, and a second, conductive hydrogen barrier film, the capacitor insulating film, and a first, conductive hydrogen barrier film are patterned in the same process.

[0023] A feature of the invention is that the capacitor insulating film may contain a ferroelectric substance material or a high dielectric constant material. The ferroelectric substance material is a ferroelectric metal oxide, such as $Pb(Zr,Ti)O_3$ and $SrBi_2Ta_2O_9$. The high dielectric constant material is a non-ferroelectric dielectric metal oxide, such as $(Sr,Ba)TiO_3$.

[0024] Numerous other features, objects and advantages of the invention will become apparent from the following description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025]

FIG. 1 is a side cross-sectional view showing a basic structure of a semiconductor device according to a first embodiment of this invention.

FIGS. 2-9 are side cross-sectional views showing a method of manufacturing the semiconductor device illustrated in FIG. 1 with each manufacturing step.

FIG. 10 is a side cross-sectional view showing a basic structure of a modified embodiment of the semiconductor device illustrated in FIG. 1.

FIG. 11 is a side cross-sectional view showing a basic structure of another modified embodiment of the semiconductor device illustrated in FIG. 1.

FIG. 12 is a side cross-sectional view showing a basic structure of still another modified embodiment of the semiconductor device illustrated in FIG. 1.

FIG. 13 shows results from measuring of hysteresis in a capacitor device portion before and after hydrogen anneal of the semiconductor device illustrated in FIG. 1.

FIG. 14 shows a frequency distribution of Vt measuring value before and after hydrogen anneal of the semiconductor device (transistor) illustrated in FIG. 1.

FIG. 15 is a side cross-sectional view showing a basic structure of a semiconductor device according to a second embodiment of this invention.

FIGS. 16-24 are side cross-sectional views showing a method of manufacturing the semiconductor device illustrated in FIG. 15 with each manufacturing step.

FIG. 25 is a side cross-sectional view showing a basic structure of a modified embodiment of the semiconductor device illustrated in FIG. 15.

FIG. 26 is a side cross-sectional view showing a basic structure of another modified embodiment of the semiconductor device illustrated in FIG. 15.

FIG. 27 is a side cross-sectional view showing a basic structure of a conventional semiconductor device in which a hydrogen barrier film is formed on an interlayer insulating film.

FIG. 28 is a side cross-sectional view showing a basic structure of another conventional semiconductor device in which a hydrogen barrier film is formed on the upper electrode of the device.

FIG. 29 is a side cross-sectional view showing a basic structure of another conventional semiconductor device in which a hydrogen barrier film is formed on the entire surface of the device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0026] By reference to the drawings, a semiconductor device and a method of manufacturing the same in several embodiments is described herein.

[0027] It should be understood that the FIGS. 1-12, 15-26 depicting integrated circuit devices in accordance with the invention are not meant to be actual plan or cross-sectional views of any particular portion of an actual integrated circuit device. In the actual devices, the layers will not be as regular and their thicknesses may have different proportions. The various layers in actual devices often are curved and possess overlapping edges. The figures instead show idealized representations which are employed to depict more clearly

and fully the method of the invention than would otherwise be possible. Also, the figures represent only one of innumerable variations of ferroelectric devices that could be fabricated using the method of the invention. For the sake of clarity, the same reference numbers have been used to identify similar elements among the different embodiments of the invention depicted in the figures.

[0028] As discussed in the problem statement above, the dielectric substance of the capacitor insulating film is an oxide that may be a ferroelectric oxide, such as $Pb(Zr,Ti)O_3$ and $SrBi_2Ta_2O_9$, or it may be a non-ferroelectric dielectric oxide, such as $(Sr,Ba)TiO_3$.

[0029] FIG. 1 is a side cross-sectional view showing a basic structure of a semiconductor device according to a first embodiment of this invention. In the structure of the semiconductor device, a device isolation oxide 2, an interlayer insulating film 6, a hydrogen barrier film 7, a lower electrode 8, a capacitor insulating film 9, an upper electrode 10, a hydrogen barrier film 11, a hydrogen barrier film 12, an interlayer insulating film 13 and a wiring layer 14 are deposited on a silicon substrate 1 with this order. The capacitor portion 19 comprising the lower electrode 8, the capacitor insulating film (dielectric film) 9 and the upper electrode 10 is completely covered with the hydrogen barrier films 7, 11, and 12. Further, a gate electrode 5 is formed on a gate oxide film 4 between impurity diffusion regions 3 in the silicon substrate 1. In this event, the characteristic of the capacitor portion 19 does not deteriorate during a manufacturing process in a reduction atmosphere after the formation of the capacitor portion 19 because the capacitor portion 19 is completely covered with the hydrogen barrier films 7, 11, and 12. Further, a MOS characteristic is effectively ensured by a hydrogen anneal, and Vt of the transistor is not fluctuated because the hydrogen barrier film is removed over the transistor.

[0030] FIGS. 2-9 are side cross-sectional views showing a method of manufacturing such a semiconductor device at the respective manufacturing steps.

[0031] First, as shown in FIG. 2, a transistor portion is fabricated by forming the gate electrode 5 on the gate oxide film 4 between the impurity diffusion regions 3 in the silicon substrate 1 by use of a known CMOS process. Thereafter, a first interlayer insulating film 6 of a BPSG layer is formed, and a first hydrogen barrier film 7 having the film thickness of 100 to 2000 Å (for example, 500 Å) is formed on the interlayer insulating film 6. The hydrogen barrier film 7 is a Si_3N_4 film that is formed by using a reduced pressure CVD method or a sputtering method. If the film thickness is less than 100 Å, the hydrogen barrier film 7 does not provide sufficient barrier performance. On the other hand, if film thickness exceeds 2000 Å, warping of the silicon substrate 1 occurs because of stress from the Si_3N_4 film. Therefore, thicknesses outside the range 100-2000 Å are undesirable. The Si_3N_4 film due to the reduced pressure CVD method is excessively dense and the content of the hydrogen is also small. Subsequently, as shown in FIG. 3, the lower electrode 8, the capacitor insulating film 9, the upper electrode 10 and a second hydrogen barrier film 11 are successively deposited on the barrier film 7. A contact layer, such as SiO_2, may be also formed between the hydrogen barrier film 7 and the lower electrode 8. For example, where a contact layer of NSG having a film thickness of 500 Å is formed on the hydrogen barrier film, a lower electrode 8 comprising a Ti film of 500 Å thickness and a Pt layer of 2000 Å thickness is deposited thereon by the use of a sputtering method. Further, the capacitor insulating film 9 having a film thickness of 2000 Å is formed by use of a sol-gel process. Thereafter, the upper electrode 10 of Pt having a film thickness of 200 Å and the hydrogen barrier film 11 of TiN having the film thickness of 500 Å are successively deposited thereon by a sputtering method. The barrier film 11 must be conductive so a conductive nitride, such as TiN and TaN, is used to form it. Further, the film thickness thereof is set to 100 Å or more to obtain a sufficient barrier performance.

[0032] Then, as shown in FIG. 4, the hydrogen barrier film 11, the upper electrode 10, the capacitor insulating film 9 and the lower electrode 8 are processed by etching.

[0033] After a third hydrogen barrier film 12 is formed on the entire upper surface, as shown in FIG. 5, the hydrogen barrier film 7 and the hydrogen barrier film 12 over the transistor are removed by etching to obtain the condition illustrated in FIG. 6. For example, the hydrogen barrier film 12 of Si_3N_4 with a thickness of 500 Å is deposited by sputtering. Then, as shown in FIG. 6, the hydrogen barrier films 7 and 12 are removed from interlayer insulating film 6, but not from the capacitor portion 19.

[0034] Further, the hydrogen barrier film 12 is formed to the same thickness using Si_3N_4 as the hydrogen barrier film 7. However, it is desirable to apply a sputtering method as the deposition method because the CVD method has a hydrogen atmosphere that deteriorates capacitance characteristics. Also, a multilayer of Si_3N_4 and SiO_2 or a film containing oxygen and nitrogen represented by SiON (namely, SiON or one selected from a group of Si_3N_4, SiON and SiO_2) is applicable for the hydrogen barrier film 12.

[0035] Next, as shown in FIG. 7, after a second insulating film 13 of SiO_2 is formed by the use of the CVD method, a contact hole is formed as shown in FIG. 8. After a W film is finally formed by the CVD method as shown in FIG. 9, W is embedded into a contact portion 20 by the etch back, and the wiring layer 14 of Al is deposited and patterned. Thereafter, the hydrogen anneal is carried out at 400°C to form a protection film on the wiring layer 14.

[0036] FIG. 10 is a side cross-sectional view showing a basic structure with respect to a modification of the semiconductor device illustrated in FIG. 1. In such a semiconductor device, a sequence for forming the

hydrogen barrier is different from the semiconductor device illustrated in FIG. 1. Namely, in this example, the second barrier film 11 is formed after the second interlayer insulating film 13 is formed and the contact hole is etched. Thereafter, the second hydrogen barrier film 11, except over the capacitor portion 19, is removed. The same structure as the semiconductor device illustrated in FIG. 1 can be obtained by the above manufacturing method.

[0037] In the structure illustrated in FIG. 1, a heat treatment of a high temperature in an atmosphere containing oxygen cannot be performed because the capacitor insulating film 9 is insulated from oxidation after the formation of the second hydrogen barrier film 11. However, the capacitance characteristic can be improved by performing an oxygen anneal after processing the capacitor insulating film 9, because the second hydrogen barrier film 11 is not formed at the same time as the capacitor insulating film 9 in this structure.

[0038] FIG. 11 is a side cross-sectional view showing a basic structure according to another modification example of the semiconductor device illustrated in FIG. 1.

[0039] In such a semiconductor device, the second hydrogen film 11 is formed after the third hydrogen barrier film 12 is formed and the contact hole of the capacitor portion 19 is etched. Thereafter, in contrast to the semiconductor device illustrated in FIG. 1, the hydrogen barrier films 11 and 12, except on the capacitor portion 19, are removed. A structure equivalent to the semiconductor device illustrated in FIG. 1 can be obtained by the above manufacturing method.

[0040] FIG. 12 is a side cross-sectional view showing a basic structure according to another modification of the semiconductor device illustrated in FIG. 1. In such a semiconductor device, in contrast to the semiconductor device illustrated in FIG. 1, the first hydrogen barrier film 7 is etched simultaneously with the lower electrode 9. A structure equivalent to the semiconductor device illustrated in FIG. 1 can be obtained by this manufacturing method.

[0041] FIG. 13 shows the result of measuring the hysteresis curve [polarization (μC/cm2) as a function of voltage(V)] of the capacitor device portion before and after the hydrogen anneal for the semiconductor device illustrated in FIG. 1. The capacitor insulating film comprised $SrBi_2Ta_2O_9$. The resulting curve shows that almost no deterioration due to the hydrogen anneal occurred.

[0042] FIG. 14 shows a frequency distribution of measured Vt-value before and after the hydrogen anneal (in the case of nMOS and pMOS transistors) for the semiconductor device illustrated in FIG. 1. It is found from the measurement results that the fluctuation of Vt after the hydrogen anneal is largely reduced.

[0043] FIG. 15 shows a side cross-sectional view showing the basic structure of a semiconductor device according to a second embodiment of this invention.

[0044] A device isolation oxide film 2, an interlayer insulating film 6 having a plug 15, a hydrogen barrier film 7, a hydrogen barrier film 11, a lower electrode 8, a capacitor insulating film 9, a hydrogen barrier film 12 and a wiring layer 14 are deposited in this order on a silicon substrate 1. In this case, a capacitor portion 19 comprising the lower electrode 8 and the capacitor insulating film (dielectric film) 9 is completely covered with the hydrogen barrier films 7, 11 and 12, and a gate electrode 5 is formed on a gate oxide film 4 between impurity diffusion regions 3 in the silicon substrate 1. In this example, in contrast to the first embodiment, the lower electrode 8 is connected to a source and a drain of a selection transistor via plug 15. As in the first embodiment, however, the capacitor portion 19 is covered with the hydrogen barrier films 7, 11, and 12, and the hydrogen barrier films, except on the capacitor portion 19, are removed. Although the capacitor portion 19 substantially overlaps the transistor portion, as shown in FIG. 15, and the hydrogen barrier films 7, 11, and 12 are located above the transistor portion, the MOS characteristic is ensured by the hydrogen anneal because the hydrogen sufficiently diffuses from the portion between the capacitor portions 19 from which the hydrogen barrier is removed.

[0045] FIGS. 16-24 are side cross-sectional views showing a method of manufacturing the semiconductor device of FIG. 15 for each manufacturing step.

[0046] First, as shown in FIG. 16, a first barrier film 7 is formed in the same sequence as the first embodiment, and as shown in FIG. 17, a contact hole is formed by the etching. Thereafter, as shown in FIG. 18, a plug 15 is formed by an etch back after polysilicon is deposited by using a CVD method.

[0047] Next, as shown in FIG. 19, the second barrier film 11 and the lower electrode 8 are deposited. TiN, TaN and the like are used as the hydrogen barrier film 11 because it must be conductive. The barrier film 11 has a film thickness of 100 Å or more to obtain sufficient barrier performance. For example, the hydrogen-barrier film 11 of TaN having a film thickness of 500 Å and the lower electrode 8 of Ru are deposited by a sputtering method.

[0048] Further, as shown in FIG. 20, lower electrode 8 and the hydrogen barrier film 11 are processed by etching, followed by formation of the capacitor insulating film 9 thereon, as shown in FIG. 21. The capacitor insulating film 9 is processed by etching, as shown in FIG. 22. For example, after the hydrogen barrier film 11 of TaN film and the lower electrode 8 of Ru layer are etched, $(Ba,Sr)TiO_3$ is formed as the capacitor insulating film 9 by a CVD method. Thereafter, the etching process is carried out.

[0049] Successively, as shown in FIG. 23, the third barrier film 12, which is conductive, is formed, and the wiring layer 14 of a plate line layer is formed thereon. For example, the hydrogen barrier film 12 of TiN having

a thickness of 500 Å is formed by the CVD method, and then polysilicon is formed as the plate line layer by CVD to obtain wiring layer 14. In this case, the CVD method used to form hydrogen barrier film 12 provides a film having excellent step coverage. In the formation of the wiring layer 14, polysilicon is formed in a reduction atmosphere in which the reaction represented by

$$SiH_4 \rightarrow Si + 2H_2$$

is performed However, the capacitor insulating film 9 is not degraded because the hydrogen barrier film 12 of TiN film is in place.

[0050] Subsequently, wiring layer 14 and hydrogen barrier films 12 and 7 are removed from between capacitor portions 19 by etching, as shown in FIG. 24. Thereafter, the second interlayer insulating film 13 and a wiring layer of Al (not shown) are formed thereon. Next, the hydrogen anneal is carried out at 400°C.

[0051] (Ba,Sr)TiO_3 of the capacitor insulating film 9 in the semiconductor device (nMOS and pMOS transistors) has a dielectric constant of about 300, and the fluctuation of Vt of the transistor is 10% or less in the case of both nMOS and pMOS

[0052] FIG. 25 is a side cross-sectional view showing a basic structure according to one modified embodiment of the semiconductor device illustrated in FIG. 15. In such a semiconductor device, the etching process after the formation of the capacitor insulating film 9 is omitted, and the capacitor insulating film 9 is etched at the same time with the wiring layer 14. Basically, the same structure as the semiconductor device illustrated in FIG. 15 can be obtained using the above manufacturing step. This semiconductor device has the advantage of reducing the manufacturing steps. On the other hand, compared to the semiconductor device depicted in FIG. 15, the semiconductor device is subjected more to the damage arising from hydrogen because the capacitor insulating film 9 is exposed at the side. However, a small degree of deterioration can be permitted because the side portion, which does not contact with the lower electrode 8, does not function in the capacitor.

[0053] FIG. 26 is a side cross-sectional view showing a basic structure according to another modified embodiment of the semiconductor device depicted in FIG. 15. In such a semiconductor device, in contrast to the semiconductor device of FIG. 15, the first hydrogen film 7 is omitted and the second hydrogen barrier film 11 is etched at the same time as wiring layer 14. Basically, the same structure as the semiconductor device illustrated in FIG. 15 can be obtained by using the above manufacturing process. In this event, although the capacitor insulating film 9 is exposed at the side surface, as in the semiconductor device of FIG. 25, this semiconductor device has the advantage that the manufacturing process can be shortened.

[0054] As described above, the deterioration of the capacitor insulating film (dielectric film) due to the hydrogen can be completely prevented, and further, excellent capacitance characteristics can be obtained in the semiconductor devices and with the manufacturing methods of this invention, despite manufacturing steps in a reduction atmosphere. Consequently, the yield can be increased as a result of increments of the operating margin. In addition, excellent capacitance characteristics can be obtained because the capacitor portion 19 is directly covered with the hydrogen barrier film. Further, the manufacturing process can be performed using a CVD method for depositing W after the formation of the capacitor portion 19, without increasing the size of the hydrogen barrier film with respect to the capacitor portion 19. Consequently, the cell area necessary for the capacitor portion 19 can be reduced, and a contact portion 20 having a high aspect ratio can be formed. In addition, the characteristic deterioration of the capacitor portion 19 with time can be prevented, and the reliability can be improved because the hydrogen barrier film has a high barrier performance for the water in addition to hydrogen.

[0055] There has been described a method for fabricating ferroelectric integrated circuits that permits exposure to hydrogen and still results in ferroelectric devices with good electrical properties. It should be understood that the particular embodiments shown in the drawings and described within this specification are for purposes of example and should not be construed to limit the invention which will be described in the claims below. Further, it is evident that those skilled in the art may now make numerous uses and modifications of the specific embodiments described, without departing from the inventive concepts. It is also evident that the steps recited may, in some instances, be performed in a different order; or equivalent structures and processes may be substituted for the various structures and processes described. Consequently, the invention is to be construed as embracing each and every novel feature and novel combination of features present in and/or possessed by the fabrication processes, electronic devices, and electronic device manufacturing methods described.

Claims

1. A semiconductor device comprising:

   a capacitor portion having a capacitor insulating film, said capacitor insulating film comprising a material selected from the group consisting of a ferroelectric substance material or a high dielectric constant material;
   a hydrogen barrier film, said hydrogen barrier film covering said capacitor portion; and
   a portion having no hydrogen barrier film.

2. A semiconductor device as in claim 1, further comprising

a transistor portion;
a surface on said capacitor portion; and
a contact portion located at said surface for electrically contacting said transistor portion to said capacitor portion, whereby said hydrogen barrier film covers said surface except for said contact portion.

3. A semiconductor device comprising:

a substrate, said substrate forming a substrate plane;
a transistor portion having a gate oxide film on said substrate, a gate electrode on said gate oxide film, and an impurity diffusion region;
a capacitor portion having a capacitor insulating film, said capacitor insulating film comprising a material selected from the group consisting of a ferroelectric substance material or a high dielectric constant material, said capacitor portion having a surface and said surface having a contact portion for electrically contacting said impurity diffusion region to said capacitor portion, said capacitor portion and said transistor portion not overlapping each other on the substrate plane; and
a hydrogen barrier film, said hydrogen barrier film located on said surface except for said contact portion;
whereby no hydrogen barrier film is located over said transistor portion.

4. A semiconductor device as in claim 3, wherein:

said capacitor portion has a top and a lower electrode, and said lower electrode has an upper surface, and said capacitor insulating film is located on said upper surface;
said semiconductor device comprises a first hydrogen barrier film, said first hydrogen barrier film being nonconductive and being located under said lower electrode and not at said contact portion;
said semiconductor device comprises a second hydrogen barrier film, said second hydrogen barrier film located on said top of said capacitor portion and said second hydrogen barrier film selected from the group consisting of conductive hydrogen barrier films and nonconductive hydrogen barrier films.

5. A semiconductor device as in claim 4, wherein said nonconductive hydrogen barrier film comprises at least one selected from the group consisting of Si_3N_4, SiON and a combination of Si_3N_4, SiON and SiO_2.

6. A semiconductor device as in claim 3, wherein:

said capacitor portion has a conductive top and a lower electrode, and said lower electrode has an upper surface and a side surface, and said capacitor insulating film is located on said upper surface and said side surface;
said capacitor insulating film has a lower surface; and
said semiconductor device comprises a nonconductive hydrogen barrier film, said nonconductive hydrogen barrier film covering said conductive top of said capacitor portion, said side surface of said lower electrode and said lower surface of said capacitor insulating film.

7. A semiconductor device as in claim 6, wherein said semiconductor device comprises a conductive hydrogen barrier film and said conductive hydrogen barrier film covers said contact portion.

8. A semiconductor device as in claim 7, wherein said conductive hydrogen barrier film comprises at least one selected from the group consisting of nitrides of Ti, Zr, Nb, Ta, Hf and W.

9. A semiconductor device as in claim 6, wherein said nonconductive hydrogen barrier film comprises at least one selected from the group consisting of Si_3N_4, SiON and a combination of Si_3N_4, SiON and SiO_2.

10. A semiconductor device as in claim 6, further comprising:

an upper electrode.

11. A semiconductor device comprising:

a substrate;
a transistor portion, said transistor portion having a gate oxide film on said substrate, a gate electrode on said gate oxide film, and an impurity diffusion region;
a plurality of capacitor portions, each of said capacitor portions having a capacitor insulating film, said capacitor insulating film comprising a material selected from the group consisting of a ferroelectric substance material or a high dielectric constant material, each of said capacitor portions formed on a plug electrically connected to said impurity diffusion region, and each of said capacitor portions having a surface with a contact portion, said contact portion being electrically connected to said transistor portion; and
a hydrogen barrier film located on said surface except for said contact portion;
whereby no hydrogen barrier film is located between said capacitor portions.

12. A semiconductor device as in claim 11 wherein:

said capacitor portion has a top and a lower electrode, and said lower electrode has an upper surface, and said capacitor insulating film is located on said upper surface;
said semiconductor device comprises a first hydrogen barrier film, said first hydrogen barrier film being nonconductive and being located under said lower electrode and not at said contact portion;
said semiconductor device comprises a second hydrogen barrier film, said second hydrogen barrier film located on said top of said capacitor portion and said second hydrogen barrier film selected from the group consisting of conductive hydrogen barrier films and nonconductive hydrogen barrier films.

13. A semiconductor device as in claim 12, wherein said nonconductive hydrogen barrier film comprises at least one selected from the group consisting of Si_3N_4, SiON and a combination of Si_3N_4, SiON and SiO_2.

14. A semiconductor device as in claim 11, wherein:

said capacitor portion has a conductive top and a lower electrode, and said lower electrode has an upper surface and a side surface, and said capacitor insulating film is located on said upper surface and said side surface;
said capacitor insulating film has a lower surface; and
said semiconductor device comprises a nonconductive hydrogen barrier film, said nonconductive hydrogen barrier film covering said conductive top of said capacitor portion, said side surface of said lower electrode and said lower surface of said capacitor insulating film.

15. A semiconductor device as in claim 14, wherein said semiconductor device comprises a conductive hydrogen barrier film and said conductive hydrogen barrier film covers said contact portion.

16. A semiconductor device as in claim 15, wherein said conductive hydrogen barrier film comprises at least one selected from the group consisting of nitrides of Ti, Zr, Nb, Ta, Hf and W.

17. A semiconductor device as in claim 14, wherein said nonconductive hydrogen barrier film comprises at least one selected from the group consisting of Si_3N_4, SiON and a combination of Si_3N_4, SiON and SiO_2.

18. A semiconductor device as in claim 14, further comprising:

an upper electrode.

19. A semiconductor device comprising:

a capacitor portion having a capacitor insulating film, said capacitor insulating film comprising a metal oxide;
a hydrogen barrier film, said hydrogen barrier film covering said capacitor portion; and
a portion having no hydrogen barrier film.

20. A semiconductor device as in claim 19, wherein said metal oxide is one selected from the group consisting of $SrBi_2Ta_2O_9$, $Pb(Zr,Ti)O_3$, and $(Sr,Ba)TiO_3$.

21. A method of manufacturing a semiconductor device comprising steps of:

forming a capacitor portion having a lower electrode, a capacitor insulating film, and an upper electrode, said capacitor insulating film comprising a material selected from the group consisting of a ferroelectric substance material or a high dielectric constant material;
forming a hydrogen barrier film that covers said capacitor portion; and
removing a portion of said hydrogen barrier film by etching.

22. A method of manufacturing a semiconductor device comprising steps of:

forming a lower electrode on a first hydrogen barrier film;
forming a capacitor insulating film on said lower electrode;
forming an upper electrode on said capacitor insulating film;
forming a second hydrogen barrier film on said upper electrode;
patterning together said first hydrogen barrier film, said lower electrode, said capacitor insulating film, said upper electrode, and said second hydrogen barrier film to form a patterned surface including a capacitor portion;
forming a third hydrogen barrier film on said patterned surface, whereby said third hydrogen barrier film is nonconductive;
removing said third hydrogen barrier film from said patterned surface, except not from said capacitor portion; and
removing a portion of said third hydrogen barrier film on said upper electrode to form a contact portion.

23. A method of manufacturing a semiconductor device comprising steps of:

forming a lower electrode on a first hydrogen barrier film;
forming a capacitor insulating film on said lower electrode;
forming an upper electrode on said capacitor insulating film;
patterning together said first hydrogen barrier film, said lower electrode, said capacitor insulating film and said upper electrode to form a patterned surface including a capacitor portion;
forming a third hydrogen barrier film on said patterned surface and removing said third hydrogen barrier film except not from said capacitor portion,
removing a portion of said third hydrogen barrier film on said upper electrode to form a contact portion, and
forming a second hydrogen barrier film to cover said contact portion, said second hydrogen barrier film being conductive.

24. A method of manufacturing a semiconductor device comprising steps of

forming a first, nonconductive hydrogen barrier film on an interlayer insulating film;
forming a plug;
forming a second, conductive hydrogen barrier film on said plug;
forming a lower electrode on said second, conductive hydrogen barrier film;
patterning said lower electrode and said second, conductive hydrogen barrier film to form a patterned surface including a capacitor portion;
forming a capacitor insulating film on said patterned surface;
removing said capacitor insulating film from said patterned surface except not from said capacitor portion;
forming a third, conductive hydrogen barrier film on said patterned surface including on said capacitor portion;
removing said third, conductive hydrogen barrier film and said first, nonconductive hydrogen barrier film from said interlayer insulating film except not from said capacitor portion.

25. A method of manufacturing a semiconductor device comprising steps of

forming a first, nonconductive hydrogen barrier film on an interlayer insulating film;
forming a plug in said first, nonconductive hydrogen barrier film and in said interlayer insulating film;
forming a second, conductive hydrogen barrier film on said plug and on said first, nonconductive hydrogen barrier film;
forming a lower electrode on said second, conductive hydrogen barrier film;
patterning said lower electrode and said second, conductive hydrogen barrier film to form a patterned surface including a capacitor portion;
forming a capacitor insulating film on said patterned surface including on said capacitor portion;
forming a third, conductive hydrogen barrier film on said patterned surface including on said capacitor portion;
removing said third, conductive hydrogen barrier film, said capacitor insulating film and said first, nonconductive hydrogen barrier film from said interlayer insulating film except not from said capacitor portion.

26. A method of manufacturing a semiconductor device comprising steps of:

forming a plug in an interlayer insulating film;
forming a first, conductive hydrogen barrier film on said plug and on said interlayer insulating film;
forming a lower electrode on said first, conductive hydrogen barrier film;
patterning said lower electrode to form a patterned surface including a capacitor portion;
forming a capacitor insulating film on said patterned surface including on said capacitor portion;
forming a second, conductive hydrogen barrier film on said patterned surface including on said capacitor portion;
removing said second, conductive hydrogen barrier film, said capacitor insulating film and said first, conductive hydrogen barrier film from said interlayer insulating film, except not from said capacitor portion.

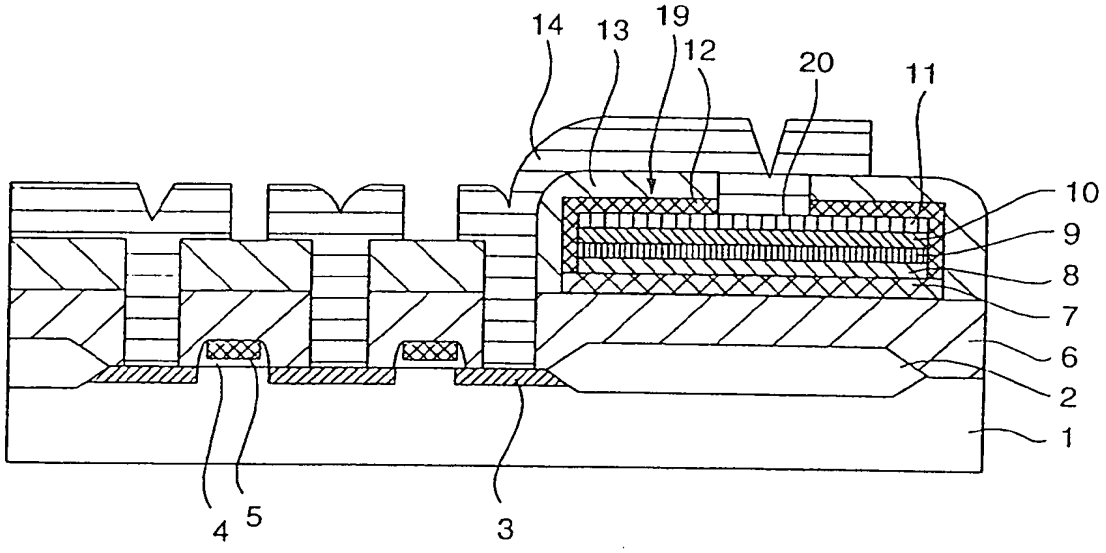


FIG. 1

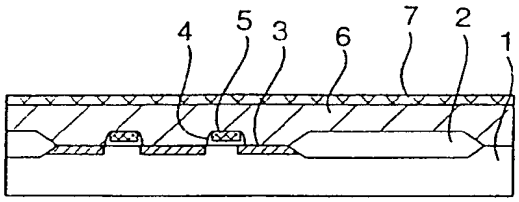


FIG. 2

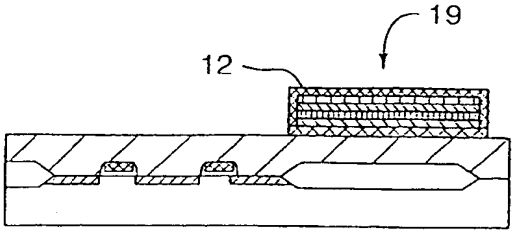


FIG. 6

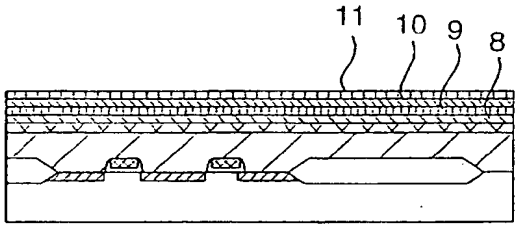


FIG. 3

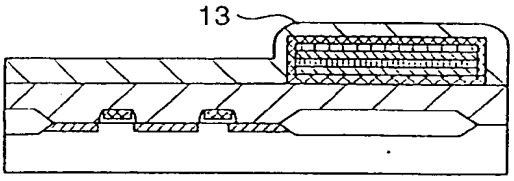


FIG. 7

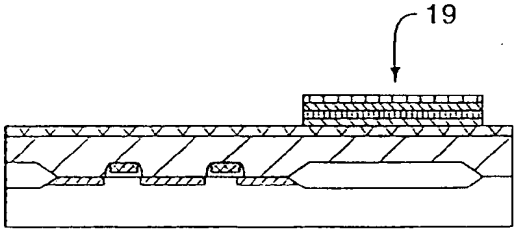


FIG. 4

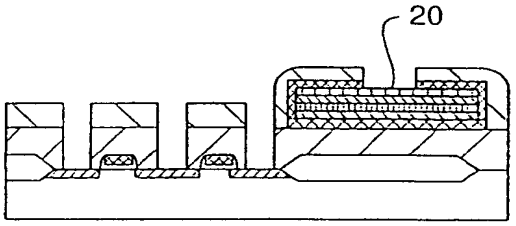


FIG. 8

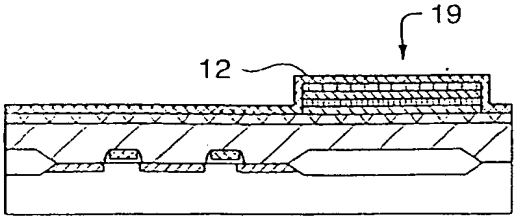


FIG. 5

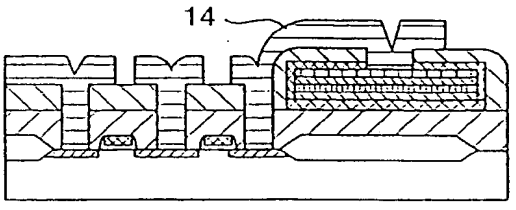


FIG. 9

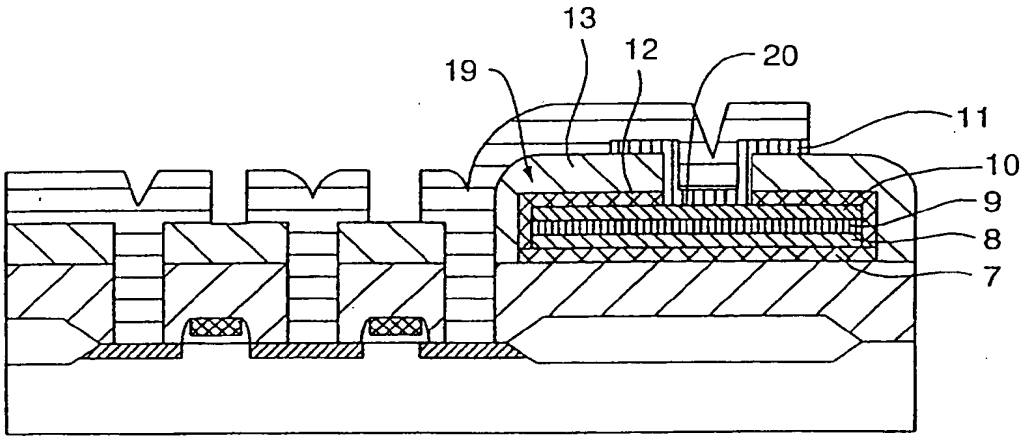


FIG. 10

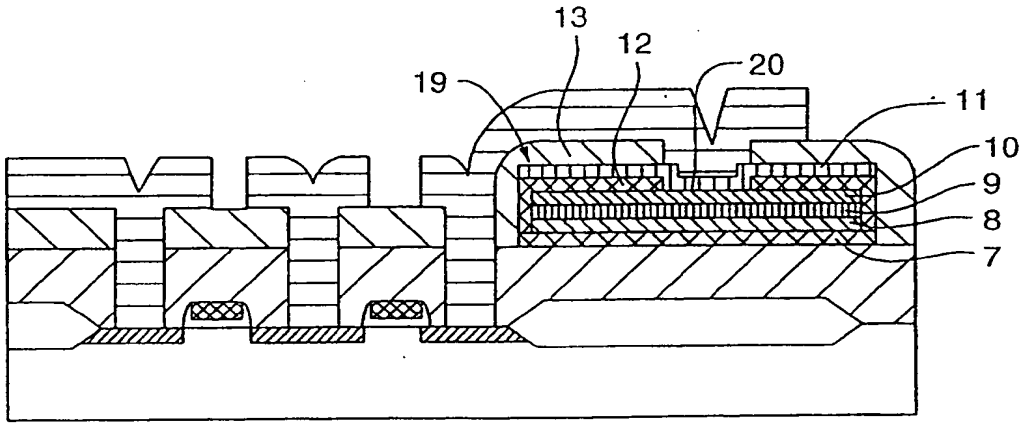


FIG. 11

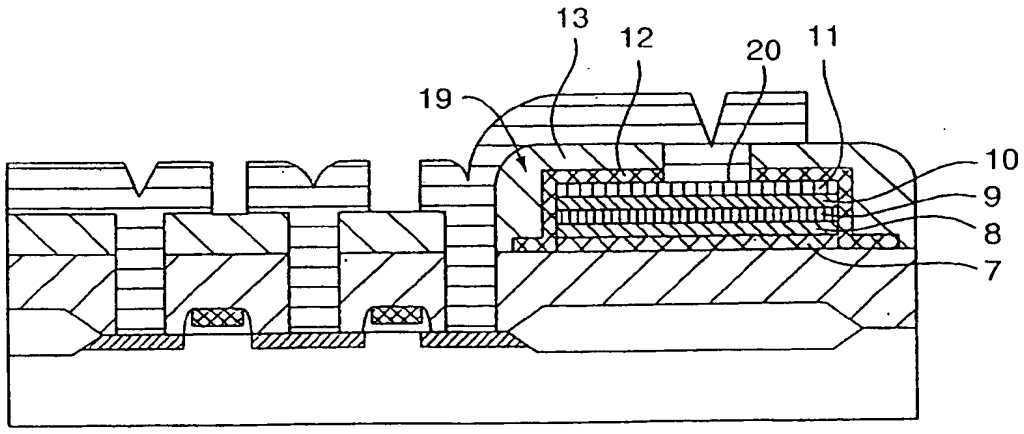


FIG. 12

FIG. 13

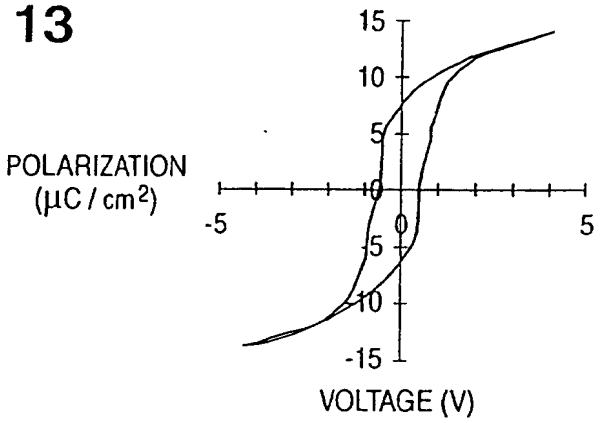


FIG. 14

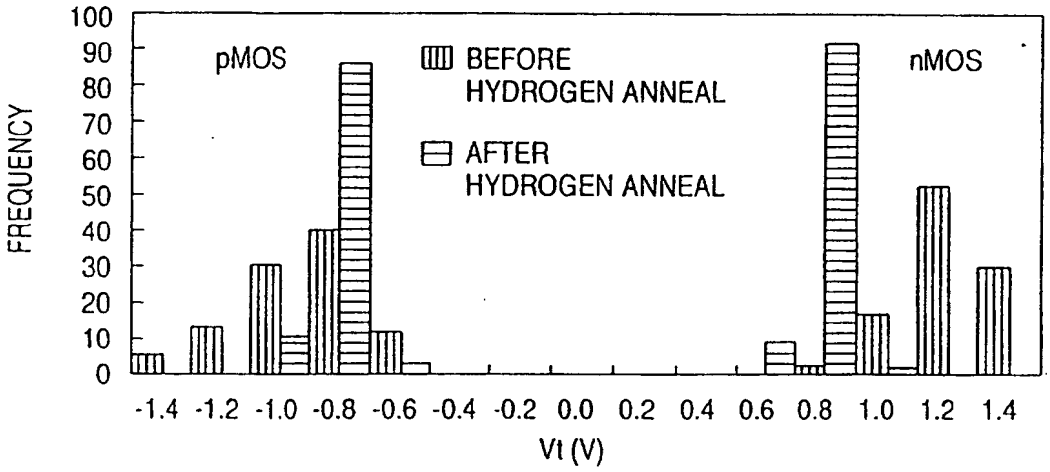
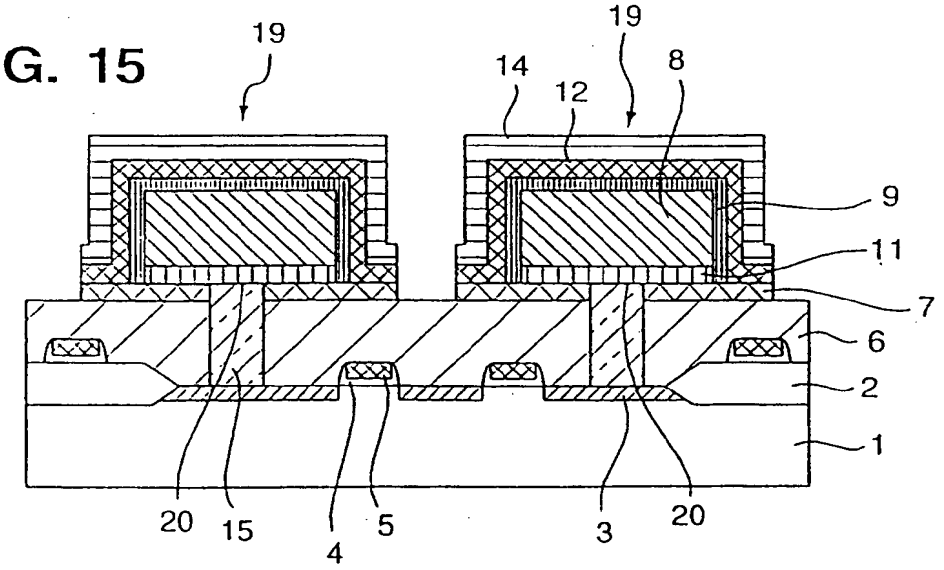


FIG. 15



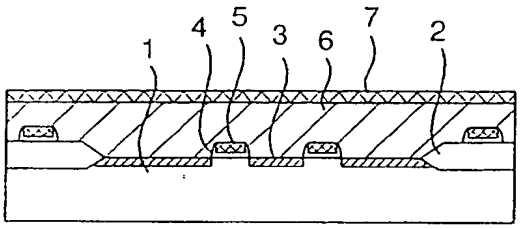


FIG. 16

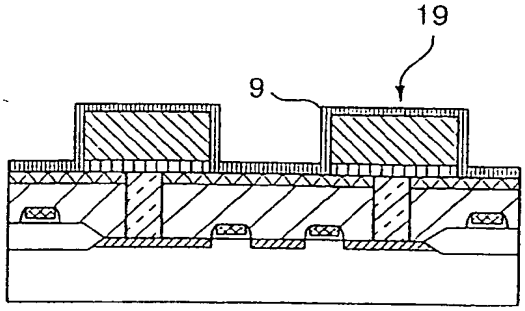


FIG. 21

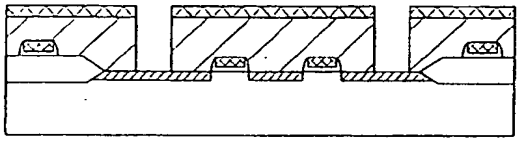


FIG. 17

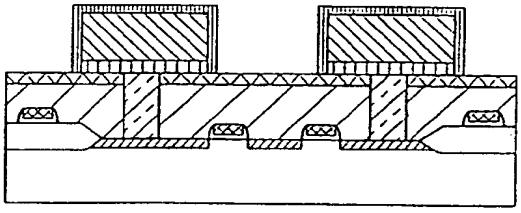


FIG. 22

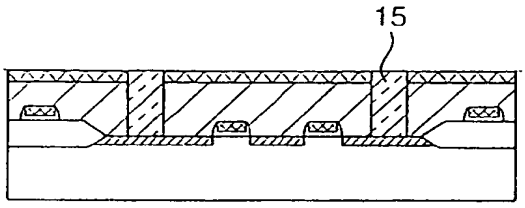


FIG. 18

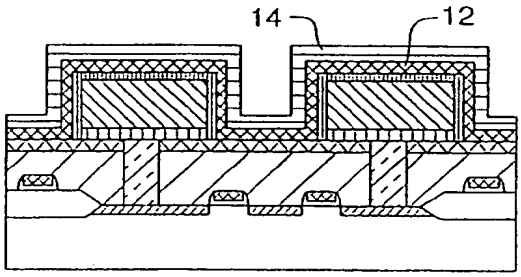


FIG. 23

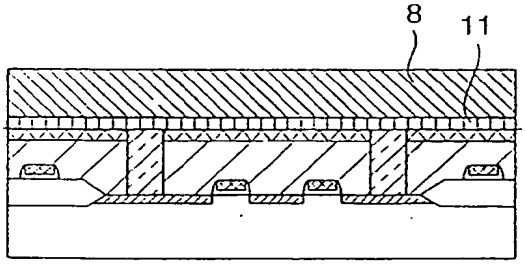


FIG. 19

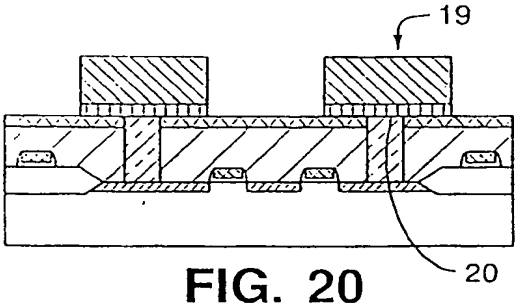


FIG. 20

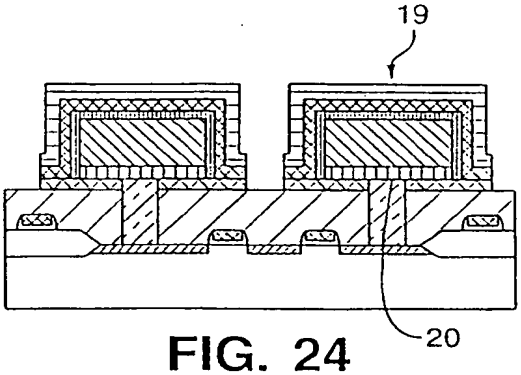


FIG. 24

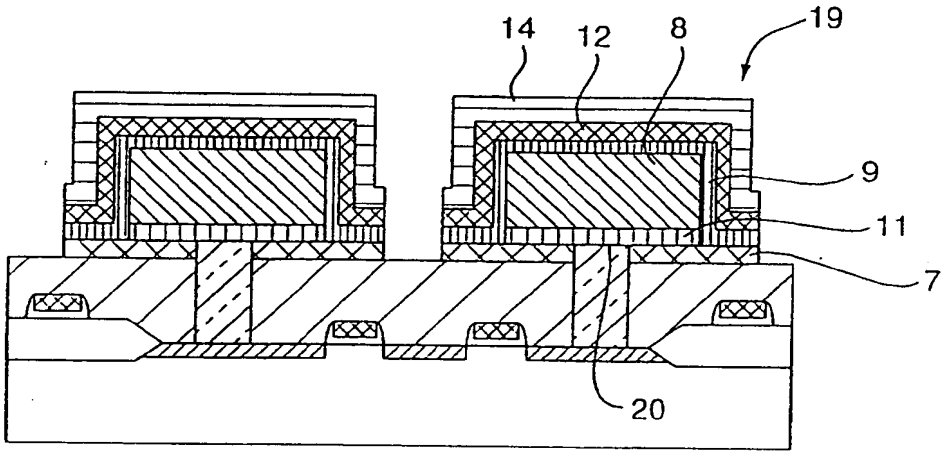


FIG. 25

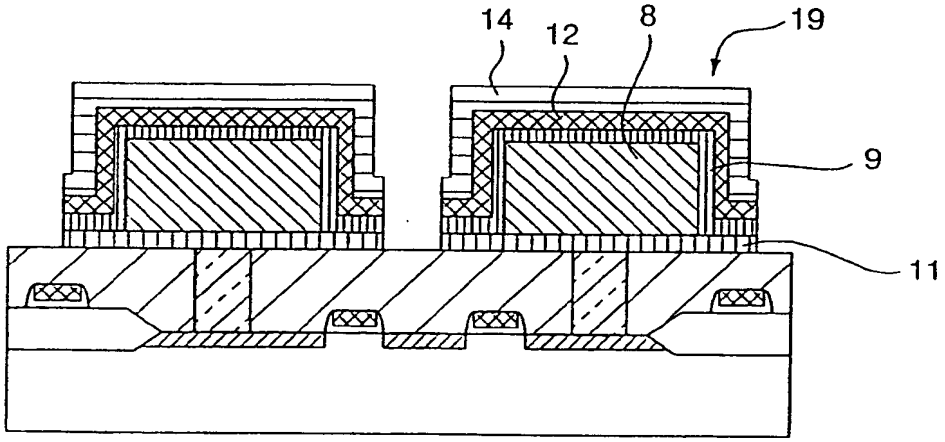


FIG. 26

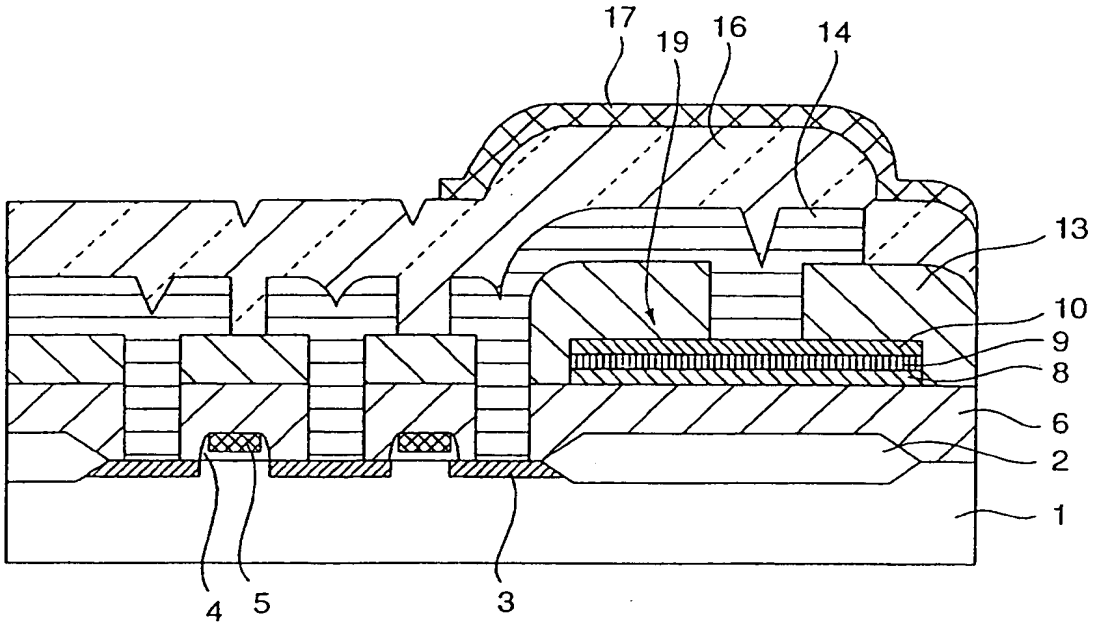


FIG. 27
PRIOR ART

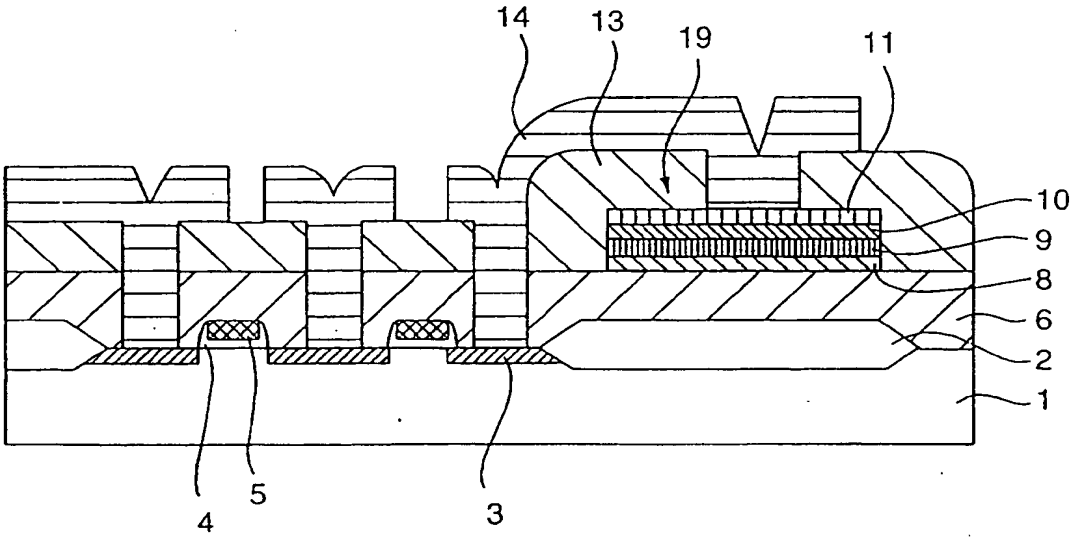


FIG. 28
PRIOR ART

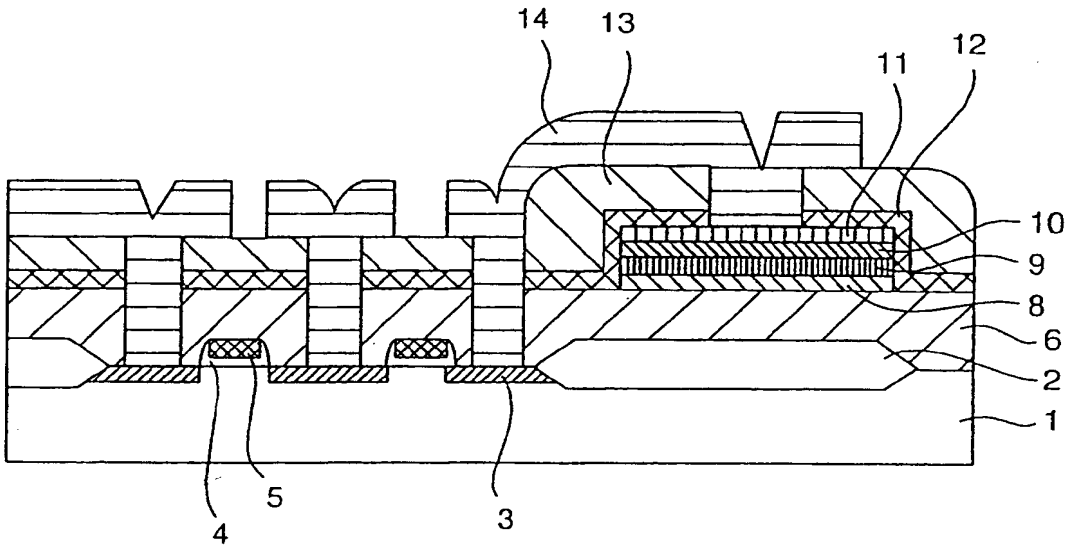


FIG. 29
PRIOR ART

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European Patent Office
Office européen des brevets

(11) EP 0 915 522 A3

(12) EUROPEAN PATENT APPLICATION

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05.01.2000 Bulletin 2000/01

(43) Date of publication A2:
12.05.1999 Bulletin 1999/19

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  Colorado Springs, CO 80918 (US)

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Postfach 26 01 62
80058 München (DE)

(54) Semiconductor device comprising a capacitor and method of manufacturing the same

(57) A semiconductor device has a device isolation oxide film (2), an interlayer insulating film (6), hydrogen barrier films (7), a lower electrode (8), a capacitor insulating film (9), an upper electrode (10), an interlayer insulating film (13) and a wiring layer (14), formed on a silicon substrate (1). A gate electrode (5) is formed on a gate oxide film (4) between impurity diffusion regions (3) in the silicon substrate (1). Further, a capacitor portion (19), comprising the lower electrode (8), the capacitor insulating film (9)(ferroelectric or high dielectric substance) and the upper electrode (10), is completely covered with the hydrogen barrier films (7,11,12). The hydrogen barrier films prevent deterioration of the ferroelectric substance and the high dielectric constant material due to reducing conditions in a hydrogen atmosphere. Other device characteristics, however, are not adversely affected because only the capacitor portion is completely covered with the hydrogen barrier films.

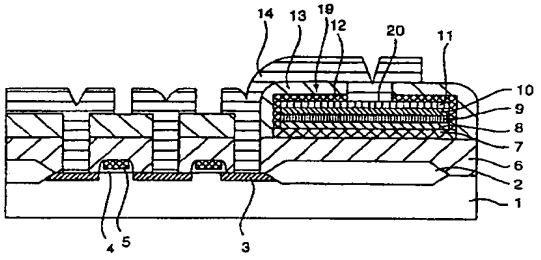

FIG. 1

EP 0 915 522 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 98 12 0416

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X A	EP 0 766 319 A (SONY CORPORATION) 2 April 1997 (1997-04-02) * the whole document *	1,21 2-4,6-8, 10-12, 14-16, 18-20, 22-26	H01L29/92 H01L21/3205
A D,A	US 5 481 490 A (WATANABE ET AL.) 2 January 1996 (1996-01-02) * column 9, line 19 - column 9, line 60 * & JP 07 111318 A (OLYMPUS OPTICAL CO LTD)	5,9,13, 17	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)
H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	5 November 1999	Baillet, B

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
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D : document cited in the application
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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 98 12 0416

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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05-11-1999

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82